REMARKS

6/17/03

Reconsideration of this application, in view of the foregoing amendments and the following remarks, is respectfully requested.

Claims 1-10 were presented for consideration in this application. By the foregoing amendment, Applicant has amended Claim 1. New Claims 11-12 have been added. Claims 1-12 are now pending.

Applicant has amended that specification to replace all "Attorney Docket No." with the current application serial number and update the status of all related applications, as requested by the Examiner. The Examiner also mentioned a reference on page 10, line16; however, Applicant finds no reference there and requests the Examiner clarify this request.

Claims 8-10 are rejected under 35 U.S.C. 102(b) as being anticipated by US 5,638,530 (Pawate et al). Claim 8 recites: "...selecting a first portion of the memory circuit responsive to a size parameter stored in a register, such that a second portion of the memory circuit is not selected; and limiting access to the first portion of memory circuit to only a first requestor of the plurality of requestors when the digital system is in a second mode of operation." Pawate has no such teaching or suggestion to select a first portion of memory in accordance with a size parameter and to limit access to the selected portion. Pawate clearly teaches that arbitration is required unless the DSP is turned off: "Since both the DSP and the host computer access the shared memory on the smart card, bus arbitration is necessary. ...If the host computer attempts to access the shared memory, the operation of the DSP is halted." (Col. 13, lines 29-35) "If the CLKON bit is set to zero, the DSP (120) is placed in a hold state, forcing the buses of the DSP (170) to be tri-stated and allowing the host computer to have free access to the common memory (150). (Col 13, lines 49-52) (See also Col 14, lines 33-36, Col 9, lines 8-14, Col 7, lines 38-42, Col 6, line 64 Col 7, line 3)

Pawate does teach use of a control register that provides limited access: "However, since the communication control and control registers are not resident in the shared memory, but in fact are resident in the interface and control circuit (180), access, write or read to these registers by the host computer does not halt the operation of the DSP." (Col 13, lines 35-39) However,

these control registers are not shared and are not relevant to the present claims. (See Col 12, lines 3-8) Therefore, Claim 8 is allowable over Pawate.

Claims 9-10 depend on allowable Claim 8 and are therefore allowable over Pawate. With respect to Claim 9, Pawate teaches: "While the smart card is in the standard mode, the DSP is inactive...." (Col 6, lines 47-49) While in smart mode, "bus arbitration is necessary." (Col 13, line 30) Thus, Pawate does not suggest a mode where a first portion of the memory is limited to one requester while the second portion is shared. Claim 9 is therefore allowable for this additional reason.

With respect to claim 10, Pawate does not teach placing the second portion of the memory circuit in a low power mode when the digital system is in the second mode of operation. Conversely, Pawate teaches "turn off the clock of the DSP" to minimize power. (Col 14, lines 6-8). Pawate does not suggest powering down a portion of the memory since the host is given access to the memory when the DSP is powered down, as discussed above. Claim 10 is therefore allowable over Pawate for this additional reason.

Claims 1-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 5,838,934 (Boutaud et al) in view of US 5,638,530 (Pawate et al)

As discussed above, Pawate has no teaching or suggestion to select a first portion of memory in accordance with a size parameter and to limit access to the selected portion, as claimed in Claim 1. Likewise, Boutaud has no such teaching. Boutaud does have a shared access mode (SAM) and a host only mode (HOM); however, the entire memory circuit 200 is treated as a single portion and is either entirely in HOM or in SAM. (Col 8, line 59 – Col 9, line 7) Neither Boutaud nor Pawate suggest "a size register for holding a size parameter coupled to the selection circuit, the selection circuit being operable to select a first portion of the memory circuit in response to the size parameter when the access mode circuitry indicates the second access mode, wherein only the first portion of the memory circuit is operable for exclusive access by the first requestor when the access mode circuitry indicates the second access mode" as recited in Claim 1, as amended. Claim 1 is amended to clarify that the size register is coupled to the selection circuit rather than connected to the memory as was erroneously recited before. Claim 1 is therefore allowable over Boutaud and Pawate in any combination.

Claims 2-7 depend directly or ultimately on allowable Claim 1 and are therefore allowable for this reason and by virtue of their further distinctive recitations. For example, with respect to claim 2, Pawate does not teach placing the second portion of the memory circuit in a low power mode when the access mode circuitry indicates the second mode of operation. Conversely, Pawate teaches "turn off the clock of the DSP" to minimize power. (Col 14, lines 6-8). Pawate does not suggest powering down a portion of the memory since the host is given access to the entire memory when the DSP is powered down, as discussed above. Claim 2 is therefore allowable over Pawate for this additional reason.

Similarly for Claim 3, since Pawate teaches: "While the smart card is in the standard mode, the DSP is inactive...." (Col 6, lines 47-49) Therefore, "a second portion of the memory circuit not selected in response to the size parameter can be accessed by the second requestor when the access mode circuitry indicates the second access mode" is not suggested by Pawate.

Regarding Claim 4, neither Pawate nor Boutaud suggest a size parameter for selecting a portion of the memory; therefore neither suggest ignoring the size parameter.

New Claims 11-12 depend on allowable independent Claim 8 and are now presented in order to more fully protect Applicant's contribution to the art.

Applicant believes this application and the claims herein to be in a condition for allowance and respectfully requests that the Examiner allow this application to pass to the issue branch.

Should the Examiner have further inquiry concerning these matters, please contact the below named attorney for Applicant.

Respectfully submitted,

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